IN THE CLAIMS:

1. (currently amended): A graphics system comprising:

one or more memories [[a memory]] configured to receive and store graphics data, wherein each [[the]] memory comprises on a single integrated chip,

one or more RAM memories [[a RAM]] configured to store the graphics data,

a level two cache memory connected to [[the]] each RAM memory, and

a level one cache memory connected to each of the level two cache [[memory]] memories;

an array of registers configured to store status information, wherein the status information tracks and indicates accesses to the graphics data in the level one cache, wherein the status information further indicates whether the graphics data is modified or unmodified; and

a memory request processor connected to the memories [[memory]] and to the array of registers, wherein the memory request processor [[controls the transfer of]] is operable to transfer graphics data from one of the level one cache memories [[memory]] to one of the corresponding level two cache [[memory]] memories according to the status information.

Sub A1

2. (original): The graphics system of claim 1, wherein the graphics data comprises samples.

3. (original): The graphics system of claim 1, wherein the graphics data comprises pixels.

4. (currently amended): The graphics system of claim 1, wherein [[the]] each level one cache memory is divided into logical blocks, and wherein each register of status information corresponds to one logical block.

5. (currently amended): The graphics system of claim 4, wherein the status information comprises:

a least recently used (LRU) count, wherein the LRU count indicates which logical block in [[the]] each level one cache memory has been least recently accessed; and

a dirty block bit, wherein the dirty block bit indicates which portions of the graphics data in [[the]] each level one cache memory has been modified.

6. (original): The graphics system of claim 1, further comprising a request queue connected to the memory request processor, wherein the request queue comprises a first-in-first-out (FIFO) storage structure, wherein the request queue is configured to receive and buffer memory requests, and wherein the request queue is further configured to output the memory requests to the memory request processor in response to control signals from the memory request processor.

Sub A1

7. (currently amended): The graphics system of claim 6, wherein the array of registers is divided into two distinct sets, wherein one set of registers stores status information indicative of a current state of [[the]] each level one cache, and wherein the second set of registers stores status information indicative of the current state of [[the]] each level one cache plus the predicted results of one or more memory requests pending in the request queue.

8. (currently amended): The graphics system of claim 1, wherein [[the]] each memory further comprises a shift register connected to [[the]] each RAM, wherein [[the]] each shift register is configured to receive and store portions of the graphics data from [[the]] each RAM, and wherein [[the]] each shift register is further configured to output graphics data serially in response to an external clock signal.

9. (original): The graphics system of claim 8, further comprising a display device, wherein the display device displays images according to the graphics data.

10. (currently amended): The graphics system of claim 1, wherein [[the]] <u>each</u> memory further comprises an arithmetic logic unit (ALU) connected to the level one cache memory, wherein the ALU is configured to:

receive as one operand graphics data from a source external to the memory;

receive as a second operand graphics data stored in the level one cache;

arithmetically combine the two operands according to a function defined by an external control signal; and

store the results of the arithmetic combination in the level one cache.

11-32. (withdrawn)

Sub A1

33. (new): A graphics system comprising:

one or more memories configured to receive and store graphics data, wherein each memory comprises on a single integrated chip,

one or more RAM memories configured to store the graphics data,

a level two cache memory connected to each RAM memory, and

a level one cache memory connected to each of the level two cache memories;

an array of registers configured to store status information, wherein the status information indicates whether the graphics data is modified or unmodified; and

a memory request processor connected to the memories and to the array of registers, wherein the memory request processor is operable to transfer graphics data from any level one cache memory to a corresponding level two cache memory if the graphics data in the level one cache memory is indicated to be modified.

34. (new): The graphics system of claim 33, wherein the transfer of graphics data is prompted on demand.

35. (new): The graphics system of claim 33, wherein the transfer of graphics data is periodic.

36. (new): The graphics system of claim 33, wherein the graphics data comprises samples.

37. (new): The graphics system of claim 33, wherein the graphics data comprises pixels.

38. (new): The graphics system of claim 33, wherein each level one cache memory is divided into logical blocks, and wherein each register of status information corresponds to one logical block.

Sub A1

39. (new): The graphics system of claim 33, wherein the memory request processor is further operable to transfer graphics data from any level one cache memory to a corresponding level two cache memory and at the same time to the RAM memory connected to the level two cache memory.

40. (new): A graphics system comprising:

one or more memories configured to receive and store graphics data, wherein each memory comprises on a single integrated chip,

one or more RAM memories configured to store the graphics data,

a level two cache memory connected to each RAM memory, and

a level one cache memory connected to each of the level two cache memories;

an array of registers configured to store status information, wherein the status information indicates whether the graphics data is modified or unmodified; and

a memory request processor connected to the memories and to the array of registers, wherein the memory request processor is operable to transfer graphics data from any level one cache memory to a corresponding level two cache memory if the graphics data in the level one cache memory is indicated to be modified and an empty memory cycle is detected.